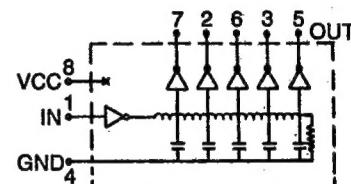
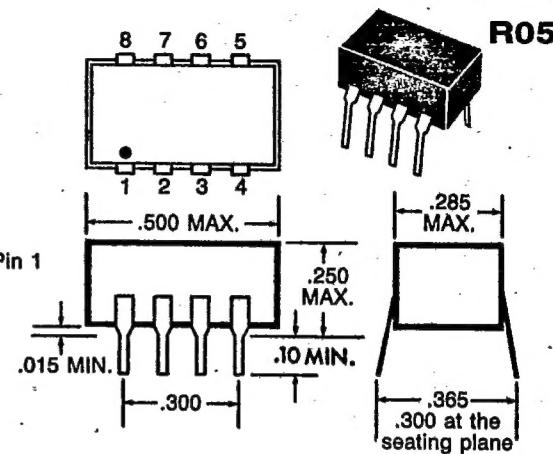
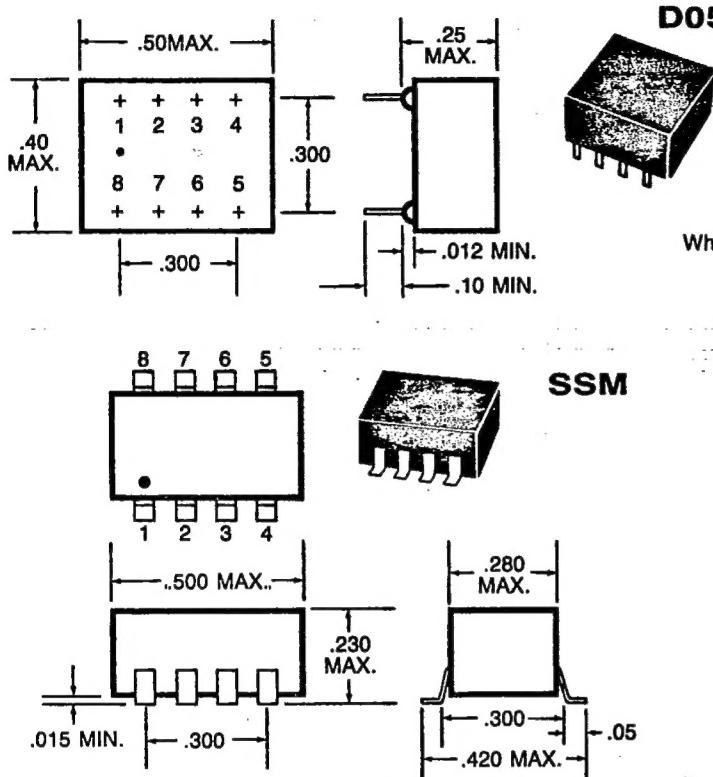


YCL

**DIL•DIP AND SURFACE MOUNTING
DIGITAL DELAY LINES
TTL COMPATIBLE
8 PIN PACKAGE**

SERIES D05, R05 AND SSM-5TAPS



MODEL NO.	TOTAL DELAY (ns)	DELAY TAP (ns)
SERIES D05	SERIES R05	SERIES SSM
D05025	R05025	SSM-05025
D05030	R05030	SSM-05030
D05040	R05040	SSM-05040
D05045	R05045	SSM-05045
D05050	R05050	SSM-05050
D05075	R05075	SSM-05075
D05100	R05100	SSM-05100
D05125	R05125	SSM-05125
D05150	R05150	SSM-05150
D05200	R05200	SSM-05200
D05250	R05250	SSM-05250
D05300	R05300	SSM-05300
D05400	R05400	SSM-05400
D05500	R05500	SSM-05500

DC PARAMETERS		LIMITS	
		Min.	Max.
Voh	Vcc = min Ioh = 1.0mA	2.5V	—
Vol	Vcc = min Iol = 20mA	—	0.5V
Ilh	Vcc = max Vlh = 2.7V	—	50 μ A
Ill	Vcc = max Vll = 0.5V	-2.0mA	—
II	Vcc = max VI = 5.5V	—	1.0mA
Vi	Vcc = min Iin = -18 modc	-1.2vdc	—
Icc	Vcc = max outputs low	—	70mA

SPECIFICATIONS:

- Supply voltage: 5.0VDC \pm 10%
- Delay tolerances: \pm 2ns or \pm 5% wig
- Minimum pulse width: 40% of Total Delay
- Maximum duty cycle: 50%
- Rise time: 4ns max
- Operating temp. range: 0°C to +70°C
- Temp. coeff. of delays: 1.0ns + 500ppm/°C
- Terminals: .020w x .010th., alloy 42

TEST CONDITIONS:

- Vcc = 5.0VDC, Temp. 25°C \pm 5°C
- Time delay measured at the 1.5V level
- Rise time measured from .75V to 2.4V
- All outputs loaded with 15pf
- Input Test Pulse:

Pulse Voltage: 3.0V
Pulse rise time: 2ns
Pulse width: 1.2 x max Td
Pulse spacing: 5 x max Td